WHAT IS CLAIMED IS:

1. A memory device comprising:

a plurality of storage means for storing information;

means for controlling said storage means;

means, having a resistance, for terminating an electric signal; and

a pattern wiring for electrically connecting said plurality of storage means, said controlling means and said terminating means;

wherein said plurality of storage means, said controlling means and said terminating means are arranged on a board, and said pattern wiring being located in a preset position on the board other than a position in which said storage means is located.

2. The memory device according to claim 1, wherein said pattern wiring is located on an insulating portion of the board surface.

3. The memory device according to claim 2, wherein said pattern wiring is arranged on a surface layer of the board for transmitting the electric signal, and the board being composed of multiple layers.

4. The memory device according to claim 3, wherein the electric signal is a signal transmitted from said controlling means to said terminating means, and an impedance of the electric signal having a preset

value.

5. The memory device according to claim 4, further comprising means for generating a clock signal, and supplying the clock signal to said storage means connected to said terminating means.

6. The memory device according to claim 5, wherein said plurality of storage means at least including:

first storage means for receiving an output signal from said controlling means, and said first storage means being arranged on a front surface of the board, and an input terminal of said first storage means facing an output terminal of said controlling means;

second storage means for receiving an output signal from said first storage means, and said second storage means being arranged on a reverse surface of the board; and

third storage means for receiving an output signal from said second storage means, and an output terminal of said third storage means facing an input terminal of said terminating means;

wherein said pattern wiring is at least arranged between said controlling means and said first storage means, between said storage means, and between said third storage means and said terminating means.

7. The memory device according to claim 5, wherein said plurality of storage means at least

including:

first storage means for receiving an output signal from said controlling means, and said first storage means being arranged to face an output terminal of said controlling means; and

second storage means for receiving an output signal from said first storage means, said second storage means being arranged to face an output terminal of said first storage means, and an output terminal of said second storage means being arranged to face an input terminal of said terminating means;

wherein said pattern wiring is at least arranged between said controlling means and said first storage means, between said storage means, and between said second storage means and said terminating means.

8. The memory device according to claim 7, wherein an input terminal of said first storage means is arranged to face the output terminal of said second storage means;

the output terminal of said first storage means is arranged to face an input terminal of said second storage means; and

wherein said pattern wiring is arranged between terminals of said first and second storage means.

9. The memory device according to claim 7, wherein only the output terminal of said first storage means and an input terminal of said second storage

means among the terminals of said first and second storage means are arranged to face each other, and said pattern wiring being arranged between said first and second storage means.

10. The memory device according to claim 7, wherein at least two of said plurality of storage means are individually provided in each of the front and reverse surfaces of the board, and said pattern wiring being connected between said storage means.

11. A socket mounting structure of a memory device comprising:

a plurality of storage means for storing information;

means for controlling said storage means;

means, having a resistance, for terminating an electric signal; and

a pattern wiring for electrically connecting said plurality of storage means, said controlling means and said terminating means;

wherein said plurality of storage means, said controlling means and said terminating means are mounted on a board, and said pattern wiring being located in a preset position on the board other than a position in which said storage means is located.

12. The socket mounting structure of the memory device according to claim 11, wherein said pattern wiring is located on an insulating portion of the board

surface between said controlling means and said terminating means.

13. The socket mounting structure of the memory device according to claim 12, wherein the electric signal is transmitted via a surface layer pattern of the board, and the board being composed of multiple layers.

14. The socket mounting structure of the memory device according to claim 13, wherein the electric signal is a signal transmitted from said controlling means to said terminating means, and an impedance of the electric signal having a preset value.

15. The socket mounting structure of the memory device according to claim 14, further comprising means for generating a clock signal, and supplying the clock signal to said storage means connected to said terminating means.

16. A mounting method of a memory device comprising:

mounting on a board a plurality of storage means for storing information;

mounting on the board a means for controlling said storage means;

mounting on the board a means, having a resistance, for terminating an electric signal; and

mounting on the board a pattern wiring for electrically connecting said plurality of storage

means, said controlling means and said terminating means;

wherein said pattern wiring is located in a preset position on the board other than a position in which said storage means is located.

17. The mounting method of the memory device according to claim 16, wherein said pattern wiring is mounted on an insulating portion of the board surface between said controlling means and said terminating means.

18. The mounting method of the memory device according to claim 17, wherein said pattern wiring is arranged on a surface layer of the board for transmitting the electric signal, and the board being composed of multiple layers.

19. The mounting method of the memory device according to claim 18, wherein the electric signal is transmitted from said controlling means to said terminating means, and an impedance of the electric signal being adjusted to have a preset value.

20. The mounting method of the memory device according to claim 19, further comprises mounting means for generating a clock signal, and supplying the clock signal to said storage means connected to said terminating means.